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Design of an Ultra Low Power Dual Slope Analog Digital Converter for UHF RFID Sensor Nodes

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Kurzfassung

In dieser Arbeit wird der gesamte Prozess der Analyse und des Entwurfs eines Dual-Slope-Analog-Digital-Umsetzer für Ultra-Low-Power-Anwendungen behandelt. Es wird gezeigt wie ein ADC mit einer Leistungsaufnahme von weniger als 300 nA bei einer Abtastrate von 1 kHz konstruiert werden kann. Erreicht wird dies durch eine iterative Optimierung der Parameter auf Transistorebene mit dem Ziel, den Stromverbrauch zu minimieren und gleichzeitig die minimale Kernfunktionalität auf dem 55 nm-Fertigungsprozess-Technologieknoten von *Global Foundries* zu gewährleisten. Der ADC ist in der Lage Eingangssignale in einem Bereich von 0 bis knapp 0,65 V in ihre digitale 11-Bit-Darstellung zu konvertieren und eine Chipfläche von 0,06 mm^2 nicht überschreiten.

Üblicherweise digital entworfene Komponenten, wie der Zähler und der Zustandsautomat wurden analog aufgebaut um den Stromverbrauch weiter zu reduzieren. Zur Überführung der logischen Komponenten des Zustandsautomaten in NAND-Gate-Logik mit Hilfe des Moor'schen Zustandsdiagramms wurde das Programm *Logisim* eingesetzt. Simulationen mit dem *Cadence* Werkzeug *ADE Assembler* wurden erstellt, um die Funktionalität für verschiedene Prozess- und Temperatur Corner sicher zu stellen und um eine Worst-Case-Analyse durchführen zu können.

Abstract

In this work the entire process of analyzing and designing a dual slope analog digital converter for ultra low power applications is covered. It shows how to construct an ADC with a power consumption less than 300 nA at a 1 kHz sampling rate. This is reached by iteratively optimizing the parameters on transistor level to minimize power consumption while assuring the minimal core functionality on the 55 nm manufacturing process technology node provided by *Global Foundries*. The ADC converts input signals in a range from 0 to almost 0,65 V to their 11 Bit digital representation while consuming a small chip area of less than 0,06 mm^2

Usually, digitally designed components like counter and state machine are constructed analogously and also optimized to further reduce power consumption. *Analog* here means that only basic components, such as transistors and resistors of the process are used and all signals are considered to be continuous. The layout is designed manually. *Digital design* on the other hand starts with logically describing the components and *synthesizing* them afterwards to generate the layout. In order to convert the state machine logical components to NAND-gate-logic from the moore state diagram a tool available online called *Logisim* was heavily used. Simulations with the *Cadence* internal tool *ADE Assembler* are made to ensure functionality for various process and temperature corners to be able to provide a worst case analysis.

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1 Introduction

As there are many standards for radio frequency communication, RFID is one of them, designed for **R**adio **F**requency **ID**entification and can be regarded as one of the next technical steps in the evolution of the classical barcode. One of the biggest advantages are the possibility to dynamically reprogram the ID of a so called RFID tag. Therefore, dynamic assignable on chip storage as well as computational power is implemented.

Characteristics of such tags are the frequency of operation and the maximum distance for communication. Since the energy used by the tag is often entirely drawn out of the electromagnetic field of the communication provided by the so called reader, no external power supply, like a battery, is needed at the tag side. Thus such a tag is called passive.

Because power consumption reduces with smaller manufacturing processes and research for ultra low power circuits is full in swing, the idea to build tags not only targeted at identification but also at implementing other integrated circuit components came up. Interestingly, the desire to include sensors gained great attention and creates the possibility to realize battery-less sensor applications. One of these might be the project SensorBIM[1]. It is part of an EU funded Interreg project by various research institutes and partner companies located in Italy and Austria. The goal is to passively meassure temperature and moisture with an UHF RFID tag in context of BIM (**B**uilding **I**nformation **M**odeling), which is a software-based method to plan buildings and support the construction and maintenance processes.

As sensing elements almost always transform analog environmental values to analog voltages or currents, but the tag's chip logic is built up digitally, a connecting component which transforms analog signals to their digital representation has to be developed, which is the scope of this work. Many types of analog-digital converters (ADC) have been researched where only a very small subgroup meets conditions for ultra low power applications, compare [1] and [7].

With a target communication range of 10 meters a maximum current consumption of about 40 µA at 1 V is allowed for the whole tag in perfect conditions [5] for an UHF RFID tag, where only 1 µA is intended to be used by the analog-digital converters and the sensors. Thus all components designed in this work must have a maximum current consumption in the sub-µ-ampere region, even when taking into account all the possible manufacturing process variations and valid operating temperature ranges.

As designing an ADC from scratch is usually not necessary, it definitely is to reach the goal of minimized overall current consumption, which is a key feature of ultra low

[1] https://www.sensorbim.eu/

power ADCs. In this special problem domain common ADC key features loose most of their importance. For example the benefit of being able to handle input signals of very high frequencies or amplitudes of a bigger range is great for universally applicable ADCs, but not needed for this application and even to avoid if it leads to higher power consumption. So the main focus while designing the ADC is on providing the required minimal functionality while keeping the current consumption as low as possible. The manufacturing process used is the 55 nm technology node provided by *Globalfoundries*.

1.1 Characteristics of Dual Slope Analog Digital Converters (DSADC)

For almost every analog-digital converter one would expect to see filter as well as sample and hold sections as preceding parts to the actual conversion component. As the appointed sampling frequency is rather high in comparison to the expected rate of change of the temperature and moisture sensor signals and the chosen ADC architecture handles higher frequencies in the input signal well due to it's integrating behavior, the filter and sample and hold sections were omitted to keep the circuits as simple as possible.

The biggest advantages of a dual slope ADC compared to other architectures in the scope if this work are listed here:

- Conversion value is independent from absolute values of R and C as it can be observed in section 3.2 when deriving the ADC equations. Furthermore, almost every component is allowed to bring in electrical deviation biases without changing the characteristics of the ADC in the scope of this work. In other words, the ADC output is robust regarding exact sizes, resistances or capacitances of the used electrical parts.
- Noise on V_{in} due to the sensors characteristics is smoothed out well due to the integrating behavior of the circuit.
- Simple structure and design. The number of parts needed for the construction are less than for other conversion principles.
- No digital analog converter is needed (like in many other approaches, i.e. Successive-approximation ADCs).

With advantages come disadvantages which are to be listed here:

- Slow. Dual slope ADC's are based on measuring the time of loading and unloading a capacitance. The longer the unload time, the more ticks a counter has to count up. With higher counter values more bits are utilized which leads to better conversion accuracy. All in all higher accuracy goes hand in hand with longer conversion times.

2 State of the art

A research group at the *Purdue University in West Lafayette, IN, USA* has frequently published papers trying to accomplish quite the same goal as this work does [12, 11]. In 2017 the group used a 130 nm process provided by *Globalfoundries*, in 2018 a 45 nm SOI (Silicon-on-Insulator) process of the same manufacturer was used.

The 1 V powered, 8 bit ADC of Shan et al. has a power consumption of 44 µW at a sampling rate of 15 kHz on the 130 nm process with an effective number of bits of about 7 using an area of 0,06 mm^2.

The 8-Bit ADC of Shan et al. accomplished a power consumption of 22 µW at a sampling rate of 30 kHz on the 45 nm SOI process with an effective number of bits of about 8 using an area of 0,04 mm^2.

In [12], as well as in [11] tables for comparisons with other researchers' results are presented, compare Table 2.1. As some of the work groups accomplished to build a whole UHF RFID tag including sensors, an ADC, the digital part and the communication frontend, the results are not entirely comparable, although they are shown to be able to categorize this work.

	Process in nm	Supply in V	Power in µW	Sample rate in s^{-1}	Area in mm^2
JSSC2010 [8]	180	0.5, 1	0.119	333	0.0416
TCAS2014 [13]	180	1	0.35	68	0.14
JSSC2015 [15] [1]	65	0.6 to 1.0	360	20000	0.0004
ISCAS2015 [3]	350	3	8		
SHAN2018 [11]	45 SOI	0.6 to 1.0	34	30000	0.04
This Work	**55**	**0.9 to 1.1**	**0.6**	**1000**	**0.058**

Table 2.1: Table taken from [11] and modified to only include columns which are of interest in regard to this work.

An ultra low power temperature sensor for food chain monitoring was implemented by [8] designed for a working range between −10 °C and 30 °C with extraordinary low power consumption and high accuracy. However, the implemented analog-digital converter is not a dual slope analog-digital converter but a less flexible method where a time difference is measured between two delay generators working mirrored in terms of tem-

[1] Sensor only, no ADC

perature sensing. They neither cover cases of higher temperature ranges, nor did they take into account the measurement of moisture.

Also [13] use the analog-digital conversion approach of [8] but come up with a slightly more complex temperature sensor unit in order to cover temperatures from $-30\,^{\circ}\mathrm{C}$ and $60\,^{\circ}\mathrm{C}$ and better linearity.

[15] even use an off chip 16 bit analog-digital converter and only present a sensing unit to generate a temperature proportional analog voltage to be measured externally with a sampling frequency of $100\,\mathrm{kS/s}$. The paper itself does not even mention RFID.

A so called RFID enabled temperature sensor for cold chain management is presented by [3] with an operation range from $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$ and a superior accuracy of $\pm 0{,}5\,^{\circ}\mathrm{C}$, while consuming around $8\,\mu\mathrm{W}$ of power. They used a dual slope converter, like [12] and [11].

As commercial teams are also working on the same topic, it's worth mentioning one of the most successful ones: `http://www.farsens.com/en/`, although it's not known how the ADC is actually implemented on their chips. Their *Rocky100 Chip* tag consumes about $10\,\mu\mathrm{A}$ without sensors.

3 Theoretical Principles

For a full understanding of which parameters the outcome of a dual slope analog-digital converter is really depending on, a theoretical analysis is necessary. ADC specifications like accuracy, conversion time and approximate chip area can easily be tweaked by changing input variables, hence, the analysis is not exclusively restricted to this work.

For future projects the entire theory part was condensed into a *Matlab* script to provide a boilerplate for designing dual slope ADCs, which is attached in the appendix as listing 1.

The following nomenclature mentions most of the used variables and describes them in short terms.

3.1 Nomenclature

Counter

$Bits$ Number of bits the counter has

$loadBits$ Number of bits the counter has to count up when loading the capacitor

$unloadBits$ Maximum number of bits the counter has to count up when unloading the capacitor

Electrical

ρ_R Ratio between R_1 and R_2

C Integrator capacitor value

I_{load} Current consumption of capacitor when loading

I_{unload} Current consumption of capacitor when unloading

R Integrator resistor value

R_1 and R_2 Resistors of the voltage divider used for deriving the integrators reference voltage level

RC Constant value for the product of the integrator's resistance and capacitance

$V_{dd_{save}}$ Maximum charging voltage for the capacitor

$V_{ref_{bias_{diff}}}$ Intended voltage gap between external and internal reference voltage

$V_{ref_{integrator}}$ Internal reference voltage

I_{bias} Bias current

V_{dd} Supply voltage

V_{ref} External reference voltage for unloading the capacitor

Time

$\rho_{loadUnload}$ Ratio of durations for loading and unloading the capacitance of the integrator

$T_{conversion}$ Maximum duration for one conversion

T_{load} Maximum duration for loading the capacitor

T_{margin} Duration between $T_{overflow}$ and T_{unload}

$T_{overflow}$ Time the counter can count at operating frequency f_0 before overflowing occurs

T_{unload} Maximum duration for unloading the capacitor

$f_{0_{raw}}$ Given externally provided oscillator frequency

$f_{0_{save}}$ Factor between raw and jitter-compensated frequency, usually a result of 2^m

f_0 Operating frequency of the counter

f_s Sampling frequency

T_{max} Sampling period

T_{pause} Time to reset the cap and read the buffer

3.2 Calculation

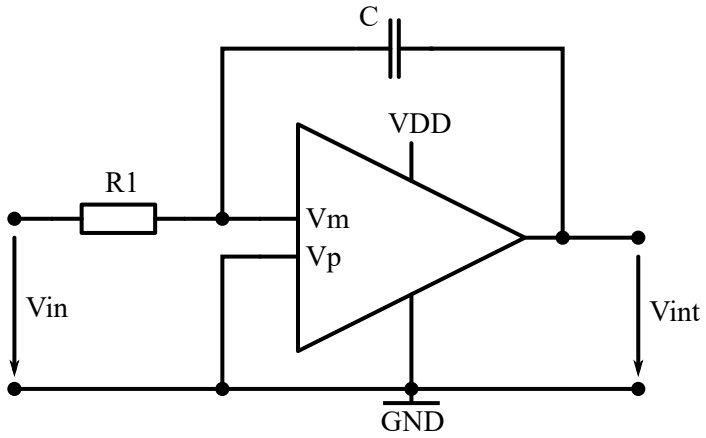

Figure 3.1: Integrator model based on an opamp operated in negative feedback loop. The capacitance causes the derivation of the feedback voltage. Hence, the opamp compares a signal with it's derivation and tries to eliminate the difference of the incoming signals. This results in integrating behavior.

As integrators for dual slope analog-digital converters are usually modeled as shown in Figure 3.1 their negative feedback loop character can be described by the following expression, [2], page 355:

$$V_{int} = -\frac{1}{RC}\int V_{in}\,dt \tag{3.1}$$

Because RC is time invariant and constant and V_{in} is expected to be quite constant and greater than zero in this project V_{int} can be shown to be linear with a constant negative slope depending on RC and being proportional to V_{in}.

$$V_{int}\big|_{V_{in}=const,RC=const} = -\frac{1}{RC}V_{in}\int dt = -\frac{V_{in}}{RC}t \tag{3.2}$$

Starting the integration from $V_{int} = 0$ with V_{in} being positive would lead to negative only values for V_{int}. V_{int}, however, is limited to positive values only due to the voltage source limitations. To increase the operating range one of the following relatively similar solutions can be chosen:

1. Preload the capacitance to a certain (well known) voltage difference to be able to unload from there.
2. Try to apply a certain (well known) voltage to the input V_p to bias the negative feedback loop deviation at the differential input stage of the operational amplifier.

Biasing the positive input of the operational amplifier is relatively easy and provides a simple way to get rid of the problem described above. Either way, a time invariant constant reference voltage is needed to be delivered from outside to the ADC component. Fortunately, the SensorBIM platform already provides a reference bandgap voltage of 0,7 V. To take into account V_{ref} Equation 3.2 has to be modified to

$$V_{int}\big|_{V_{in}=const,RC=const} = -\frac{1}{RC}\left(V_{in} - V_{ref}\right)\int dt = -\frac{V_{in} - V_{ref}}{RC}t \tag{3.3}$$

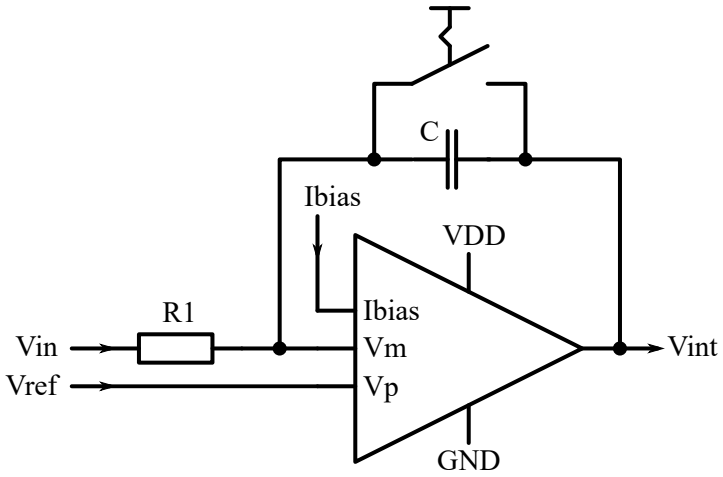

Figure 3.2: Model of an integrator resetting approach realized with a momentary switch. The bias current I_{bias} is needed inside the operational amplifier as a source to drive internal current mirrors which aim at reductions of the overall current consumption of the operational amplifier.

To reset the integrator a method to instantly discharge the capacitance is implemented to ease out the voltage drop over C. The switch model in Figure 3.2 is implemented as a PMOS transistor controlled by an external signal like shown in Figure 3.3.

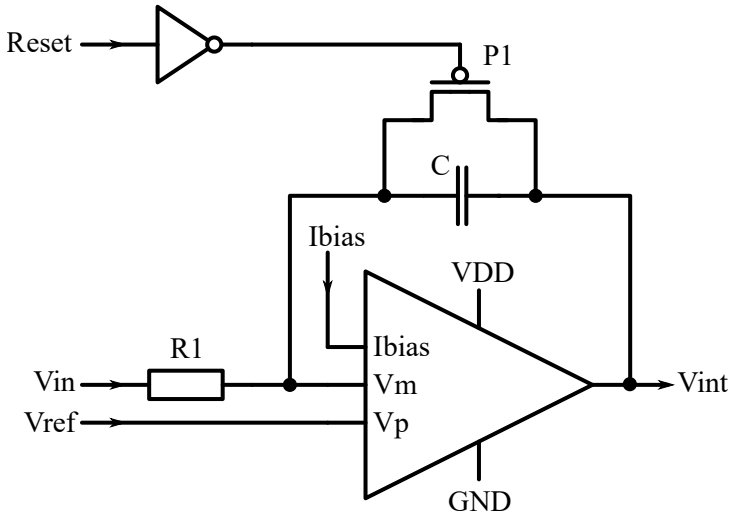

Figure 3.3: Integrator block as it's implemented in the original layout on the SensorBIM IC. A PMOS transistor is used as switch. The external reference voltage is expected to be 0,65 V. If the *Reset* signal is high, the PMOS gate is low ($GND = 0$). The nominal operating voltage of V_m is 0,65 V due to the feedback loop trying to counter the voltage difference between V_m and V_p. The operating range for V_{int} reaches from 0,65 V to 1 V. The source gate voltage difference therefore always is between 0,65 V and 0,9 V which is greater than the threshold voltage. Hence, the PMOS transistor is fully conductive. If the *Reset* signal is low, the PMOS gate is high ($V_{dd} \approx 1$ V). The source gate voltage difference therefore always is between $-0{,}35$ V and $-0{,}1$ V which is smaller than the threshold voltage. Hence, the PMOS transistor is non conductive.

To study the behavior of the circuit for the two switch positions the following cases should be considered. The transient case is not considered here.

1. Switch open: The static equivalent circuit diagram is shown in Figure 3.4. This results in the yet to analyze integrator.

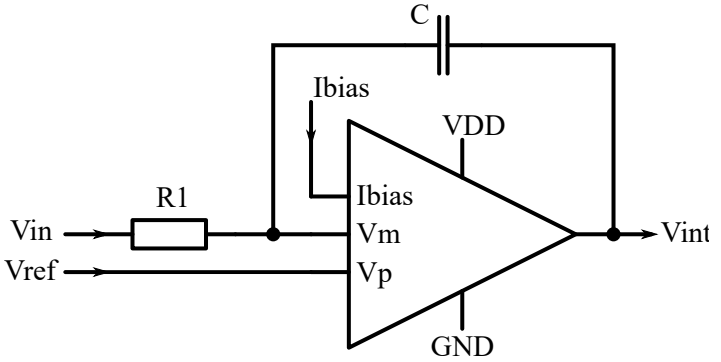

Figure 3.4: Result of Figure 3.2 when the switch is open, the integrator.

2. Switch closed: The static equivalent circuit diagram is shown in Figure 3.4. In fact the result is an impedance converter. Besides that, the capacitance is discharged

immediately due to the indirectly conducting connection between it's two ports.

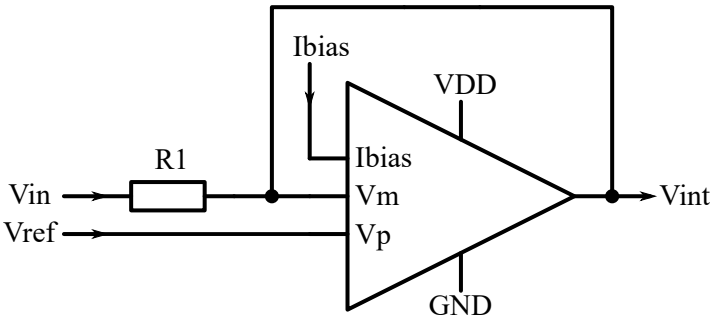

Figure 3.5: Result of Figure 3.2 when the switch is closed, an impedance converter, hence,V_{int} follows V_{in}.

3.3 Specifications

As multiple partner companies are part of the project specification restrictions came up while discussing and evaluating the needs of each participant. Compromises were made and results have settled as follows for the categories *Time* and *Electrical*.

Time

The maximum conversion time should not extend one millisecond. It's reciprocal value is the sampling frequency f_s. The externally provided on chip ring oscillator frequency origins from a separate component based on [10], which is not shown in this work.

$$f_s = 1\,\text{kHz} \tag{3.4}$$
$$f_{0_{raw}} = 2{,}1\,\text{MHz} \tag{3.5}$$

If jitter compensation is needed a value other than 1 can be set for $f_{0_{save}}$. This would result in averaging impulse times, a smaller input frequency and therefore reduced counter resolution.

$$f_{0_{save}} = 1 \tag{3.6}$$
$$f_0 = \frac{f_{0_{raw}}}{f_{0_{save}}} = 2{,}1\,\text{MHz} \tag{3.7}$$

After finishing conversion a maximum timespan to read out the counter value and reset the ADC components has to be taken in account and is estimated as a fraction of the entire conversion time.

$$T_{max} = \frac{1}{f_s} = 1\,\text{ms} \tag{3.8}$$
$$T_{pause} = \frac{1}{10} T_{max} = 0{,}1\,\text{ms} \tag{3.9}$$

Electrical

V_{dd} and V_{ref} are provided externally to the ADC, hence, they are determined by other chip components. As the exact value of V_{dd} is not as critical (already taken care of with $V_{dd_{save}}$ from Equation **??**), variations of V_{ref} are seriously affecting the ADC output voltage.

$$V_{dd} = 1\,\text{V} \tag{3.10}$$
$$V_{ref} = 0{,}7\,\text{V} \tag{3.11}$$

Inside the ADC V_{ref} is used as the integrator unloading voltage as well as for deriving the reference voltage $V_{ref_{integrator}}$ used by the integrator and comparator components.

$$V_{ref_{bias_{diff}}} = 0{,}05\,\text{V} \tag{3.12}$$
$$V_{ref_{integrator}} = V_{ref} - V_{ref_{bias_{diff}}} = 0{,}65\,\text{V} \tag{3.13}$$

3.4 Analysis

From the specifications stated above the remaining interesting values are calculated separated in categories *Time*, *Electrical* and *Counter*.

Time

$$T_{conversion} = T_{max} - T_{pause} = 0{,}9\,\text{ms} \tag{3.14}$$

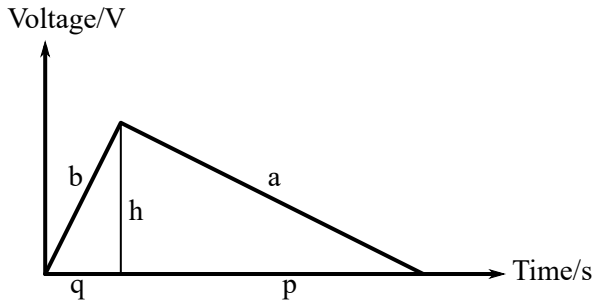

Figure 3.6: Model of the loading and unloading behavior of a dual slope analog digital converter. The slopes of b and a are indirectly proportional to the associated times q and p.

From Equation 3.2 as well as from the simulation results in Figure 5.2 a model that's shown in Figure 3.6 can be derived to help understanding how time restrictions for loading and unloading are found. q and p as well as their ratio $\rho_{loadUnload}$ can be calculated consequently. For the slopes of b and a Equation 3.2 has to be taken into account, which states, that as long as RC and V_{in} are constant in time, V_{int} is linear. Hence the slope is constant and evaluable to

$$\frac{dV_{int}\big|_{V_{in}=const,RC=const}}{dt} = -\frac{V_{in} - V_{ref}}{RC} \tag{3.15}$$

In consequence the ratios $\frac{h}{q}$ and $\frac{h}{p}$ can be directly brought into context with their associated V_{in} parameterized slopes. The limits of V_{in} which are $V_{in_{max}} = 0{,}7\,\text{V}$ and $V_{in_{min}} = 0$ are taken to evaluate the ratios.

$$\frac{h}{q} \widehat{=} -\frac{V_{in} - V_{ref}}{RC}\Big|_{V_{in}=V_{in_{min}},V_{ref}=0{,}65\,\text{V}} = \frac{0{,}65\,\text{V}}{RC} \tag{3.16}$$

$$\frac{-h}{p} \widehat{=} -\frac{V_{in} - V_{ref}}{RC}\Big|_{V_{in}=V_{in_{max}},V_{ref}=0{,}65\,\text{V}} = \frac{-0{,}5\,\text{V}}{RC} \tag{3.17}$$

$\rho_{loadUnload}$ evaluates to the ratio of the calculated slopes.

$$\rho_{loadUnload} = \frac{q}{p} = \frac{h}{p}\frac{q}{h} = \frac{0.5}{0.65} = \frac{1}{13} \approx 0.0769 \tag{3.18}$$

With $\rho_{loadUnload}$ the concrete load and unload times can now be calculated.

$$T_{load} = \frac{T_{conversion}}{\frac{1}{\rho_{loadUnload}+1}} \approx 64{,}29\,\mu s \tag{3.19}$$

$$T_{unload} = T_{conversion} - T_{load} \approx 835{,}71\,\mu s \tag{3.20}$$

$$\tag{3.21}$$

Electrical

To prepare for unforeseen voltage source drops and to prevent the integrator from trying to load up the capacitance above V_{dd} a voltage margin has to be set. As the chip and, hence, the ADC should also work with a voltage source of 0,9 V the margins width results to 0,1 V.

$$V_{dd_{save}} = V_{dd} - 0{,}1\,V = 0{,}9\,V \tag{3.22}$$

$$\tag{3.23}$$

From the load time and with Equation 3.2 RC can be computed.

$$RC = T_{load}\frac{V_{ref_{integrator}}}{V_{dd_{save}} - V_{ref_{integrator}}} = 167{,}14\,\mu\Omega\,F \tag{3.24}$$

Setting R to a value which serves an electrical component not too big in dimensions results in a concrete value for C. Values for the resistance and the capacitance can be chosen almost arbitrary, because they have no effect on the conversion time, which can be observed in Figure 5.2 or Equation 3.4.

$$R = 10\,M\Omega \tag{3.25}$$

$$C = \frac{RC}{R} = 16{,}714\,pF \tag{3.26}$$

In order to be able to derive the integrators $V_{bias_{integrator}}$ reference voltage from the external reference voltage V_{ref} a voltage divider is used. A maximum current consumption as well as the voltage ratio of the reference voltages are given.

$$I_{max} = 50\,nA \tag{3.27}$$

$$\rho_R = \frac{V_{ref_{bias_{diff}}}}{V_{ref_{integrator}}} \approx 0.0769 \tag{3.28}$$

V_{dd} is chosen here instead of V_{ref} to be sure to never exceed I_{max}, even if the reference voltage V_{ref} has to be adapted in the future.

$$R_1 = V_{dd}\frac{\rho_R}{I_{max}(1+\rho_R)} \approx 1{,}4286\,M\Omega \tag{3.29}$$

$$R_2 = \frac{R_1}{\rho_R} = 18{,}571\,M\Omega \tag{3.30}$$

The nominal loading and unloading currents can be calculated using ohms law and the maximum voltage differences occurring.

$$I_{load} = \frac{V_{ref_{integrator}} - 0}{R} = 65\,nA \tag{3.31}$$

$$I_{unload} = -\frac{V_{ref_{bias_{diff}}}}{R} = -5\,nA \tag{3.32}$$

Counter

For the counter dimensioning the minimum number of bits can be derived from the longest time the counter has to measure and the externally provided operating frequency. For the discrete counter construction the calculated minimum number of bits is rounded up.

$$loadBits = \log_2(T_{load} f_0) = 7.0768 \tag{3.33}$$

$$unloadBits = \log_2(T_{unload} f_0) = 10.7773 \tag{3.34}$$

$$bits = \lceil unloadBits \rceil = 11 \tag{3.35}$$

To show the successful prevention regarding a counter overflow while unloading the time margin can be calculated.

$$T_{overflow} = 2^{Bits} \frac{1}{f_0} = 975{,}24\,\mu s \tag{3.36}$$

$$T_{margin} = T_{overflow} - T_{unload} = 139{,}52\,\mu s \tag{3.37}$$

4 Design

For other technology nodes research already is done (compare [4, 14] for example), although most of the publications don't show detailed schematics or how they achieved minimizing the current consumption, if they even do (compare [3, 6, 9]). Other than that at least two publications exist [11, 12] with the associated schematics published. With their goal set to aim for 30 kS/second, they had an ADC power consumption of about 22 µW with a supply voltage of 1 V at the 45 nm SOI technology node from *Globalfoundries*.

4.1 Overview

This section provides an assembled overview of the implemented components that are used in this work and partially shown in this chapter:

- Counter
- State Machine
- Integrator
- Multiplexer, abbreviated to mux
- Comparator
- Voltage divider consisting of R_1 and R_2 shown in Figure 4.1.

All the components are designed analog. While some of them have to be, others, the counter and the state machine to be precise, may be replaced by their digital counterparts in the future.

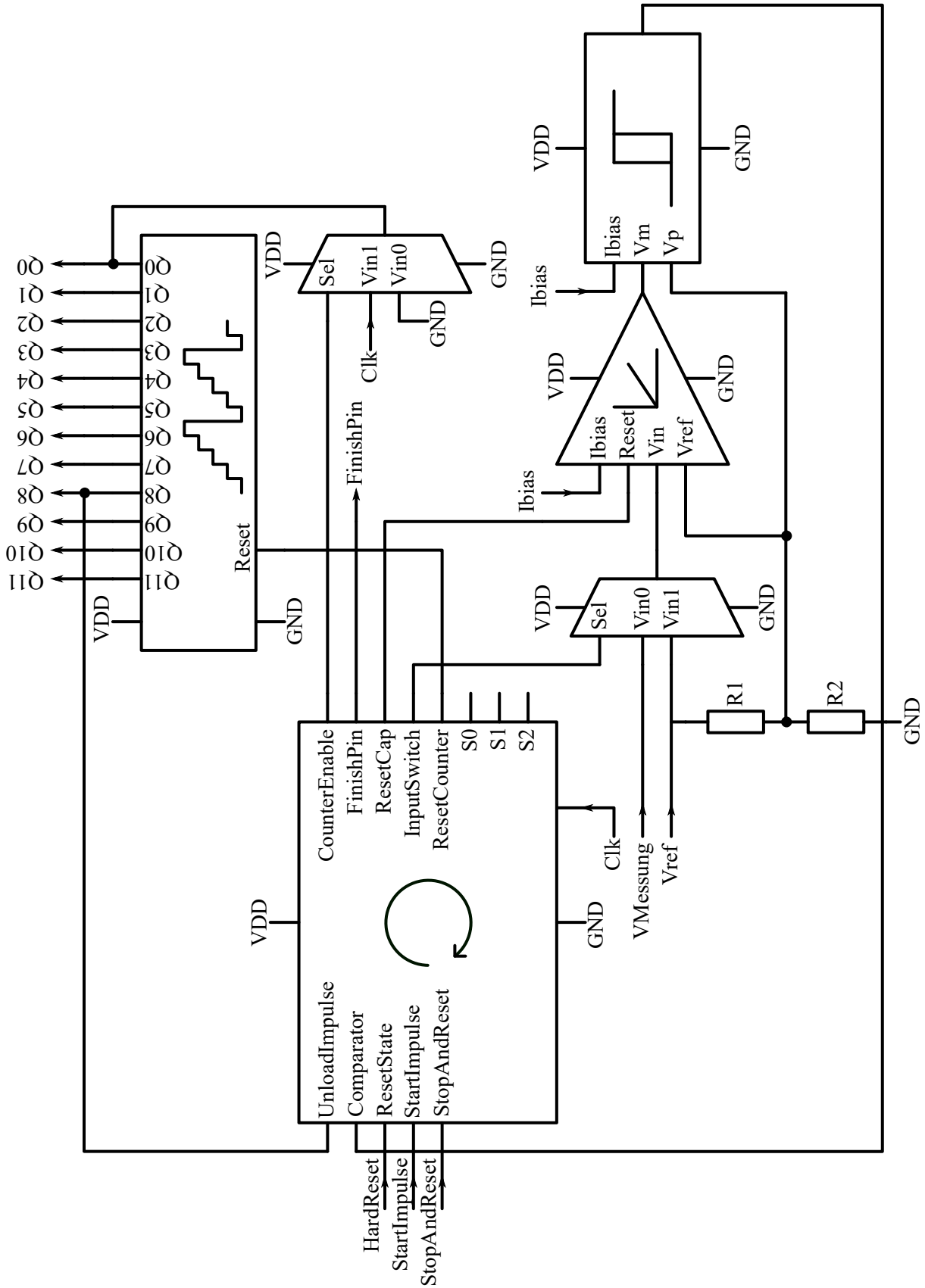

Figure 4.1: Schematics of the assembled ADC components. The counter's detail schematics are in Figure 4.8 and the opamp's detail schematics in Figure 4.7.

Although it's planned to also implement digital circuit parts on the final chip that will substitute some of the subcomponents shown, as the counter for example, it's a major requirement of this work to be able to run the ADC in standalone mode for testing and functional verification purposes. The comparator is entirely covered by another authors master thesis [5] for which reason it's not included here.

4.2 Components

State Machine

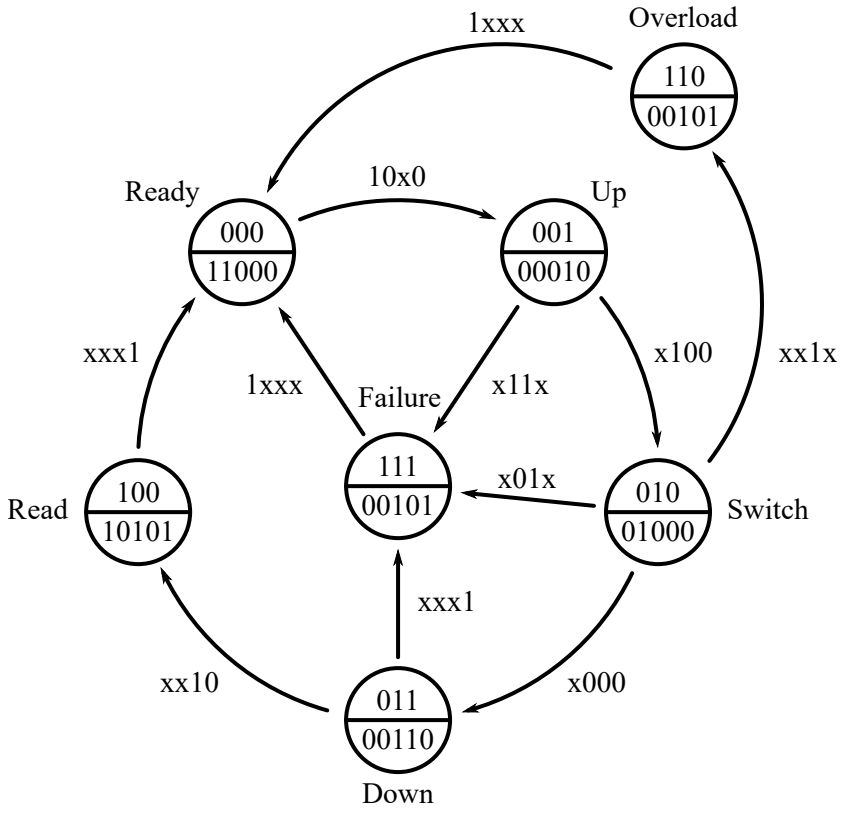

Figure 4.2: Depiction of the designed finite state diagram for managing the various states of the ADC. Based on this diagram truth Tables 1 and 2 are derived to be able to further derive the NAND gate logics presented in Figures 4.4, 4.5 and 4.6.

The finite state moore machine is designed manually in form of a finite state diagram, like shown in Figure 4.2 and mathematically described as the truth table presented in Tables 1 and 2. It has 7 states and thus 3 bit state storage is sufficient. Its implementation needs 3 flipflops.

The four input bit names in order from left to right are

1. StartImpulse
   has to be triggered externally to start the conversion or, if automatic conversion is desired, it has to be set to always high.
2. BitQ9
   is triggered as soon as the counter's 9^{th} bit goes high, respectively when the load time is over.
3. Comparator
   is directly connected to the comparator's output and usually stops the counter.
4. StopAndReset
   can be triggered externally to change from „Read“ to „Ready“ state.

The five output bit names are

1. ResetCap
   resets the integrators capacitance and therefore resets the integrator
2. ResetCounter
   resets all counter bits. This usually occcurs when changing to „Ready“ state
3. InputSwitch
   provides the mux's input signal to switch between measured input and reference voltage
4. CounterEnable
   provides the mux's input signal to switch between clock signal and ground. This enables the ADC to avoid wasting dynamic switching current when not needed.
5. FinishPin
   serves external components with the information that a conversion is finished. This usually happens with changing to the „Read“ state.

After starting up, the state machine should be in „Ready“ or „Read“ state. Assumed that it's in ready state a typical conversion starts with the StartImpulse applied externally. It's pulse width should be at least twice the clock signal period. The state machine changes into the „Up“ state which enables the counter and stops resetting the integrator's capacitance. As soon as the 9^{th} bit of the counter goes high, uploading time is over and the machine switches to the „Switch“ state, which resets the counter and immediately switches to the „Down“ state as soon as BitQ9 is low again. From there on the counter is counting up again. This is because the reference voltage is applied as input voltage instead of the measured voltage due to the states output switching the InputSwitch pin to high. After waiting for the comparator to report that the integration voltage passed the reference voltage level the machine's state immediately switches to „Read“ in which external components can take their time to read out the counter value before telling the state machine to go back to the initial state by sending a StopAndReset high impulse. The overload state is entered out of the „Switch“ state if the comparator is triggered before unloading has even begun. This happens when the measured voltage was higher than the reference voltage.

Connections between input and output stages as well as the state saving mechanism can be seen in Figure 4.3.

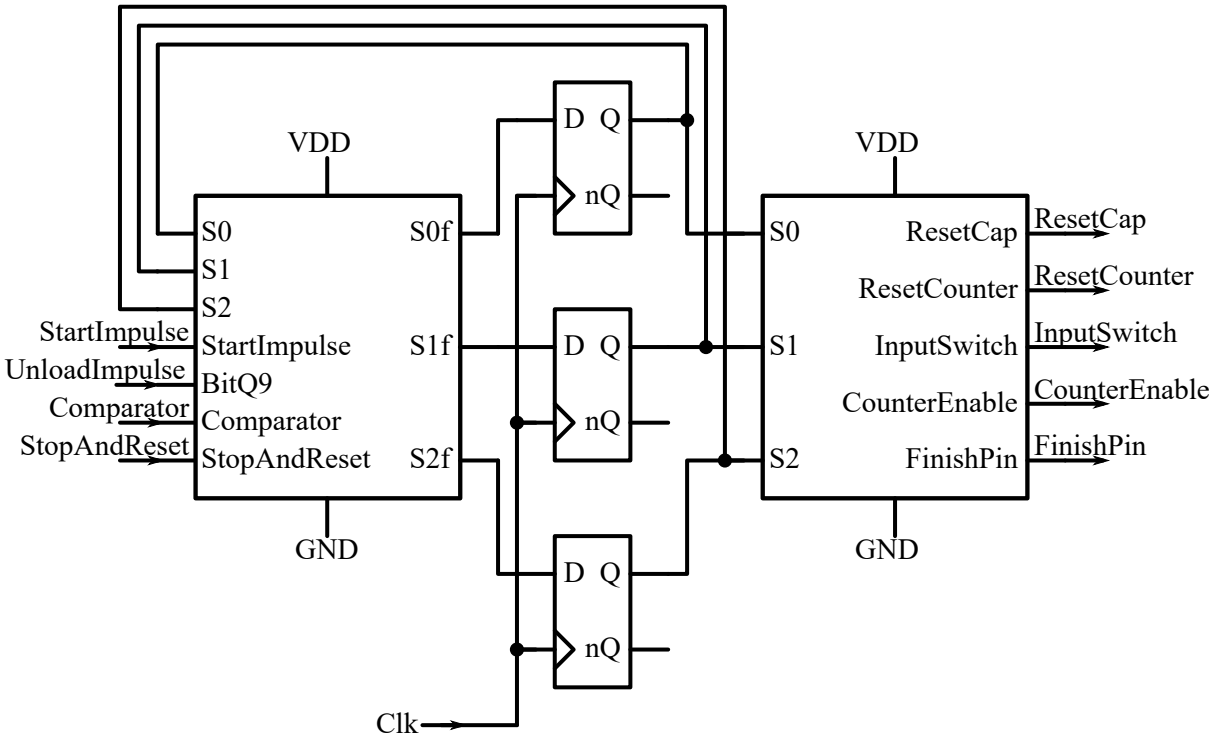

Figure 4.3: State machine split up into an internal logic, a unit for state persistence (D-flipflop array, one flipflop for each of the state bits *S*0, *S*1, *S*2), and an output logic component (shown in order from left to right). Input and output stages are realized as NAND gate logic and shown in Figures 4.4, 4.5 and 4.6.

To build up the NAND gate based logic components truth tables based on the finite state machine diagram are derived by hand (compare Table 1). With the help of a piece of software called *Logisim* [1] the truth tables are converted to logical expressions, minimized afterwards and converted to the NAND gate logic of Figures 4.4, 4.5 and 4.6 which then are wrote off to the final *Cadence Virtuoso* schematics.

[1] http://www.cburch.com/logisim/de/index.html

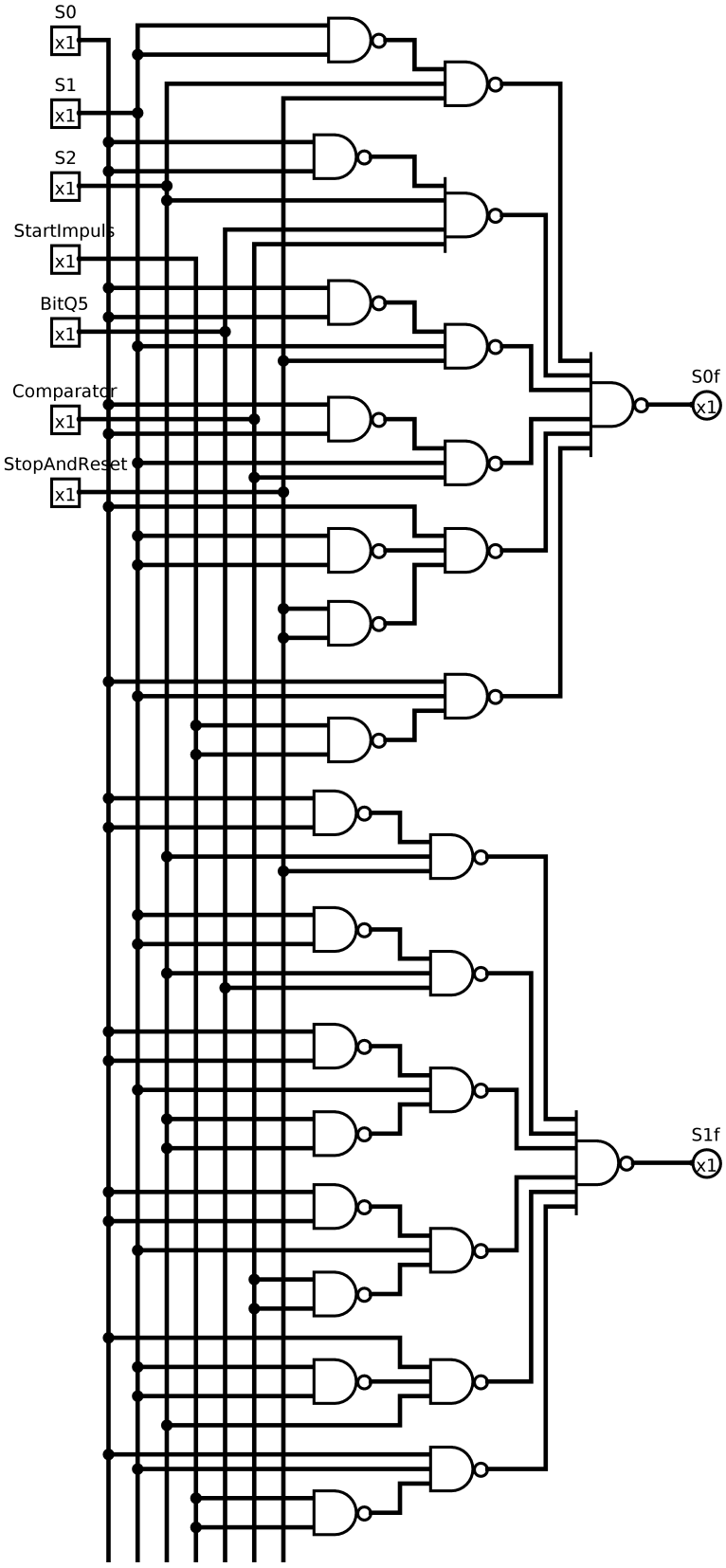

Figure 4.4: NAND gate realization of the input logic. To be continued by 4.5

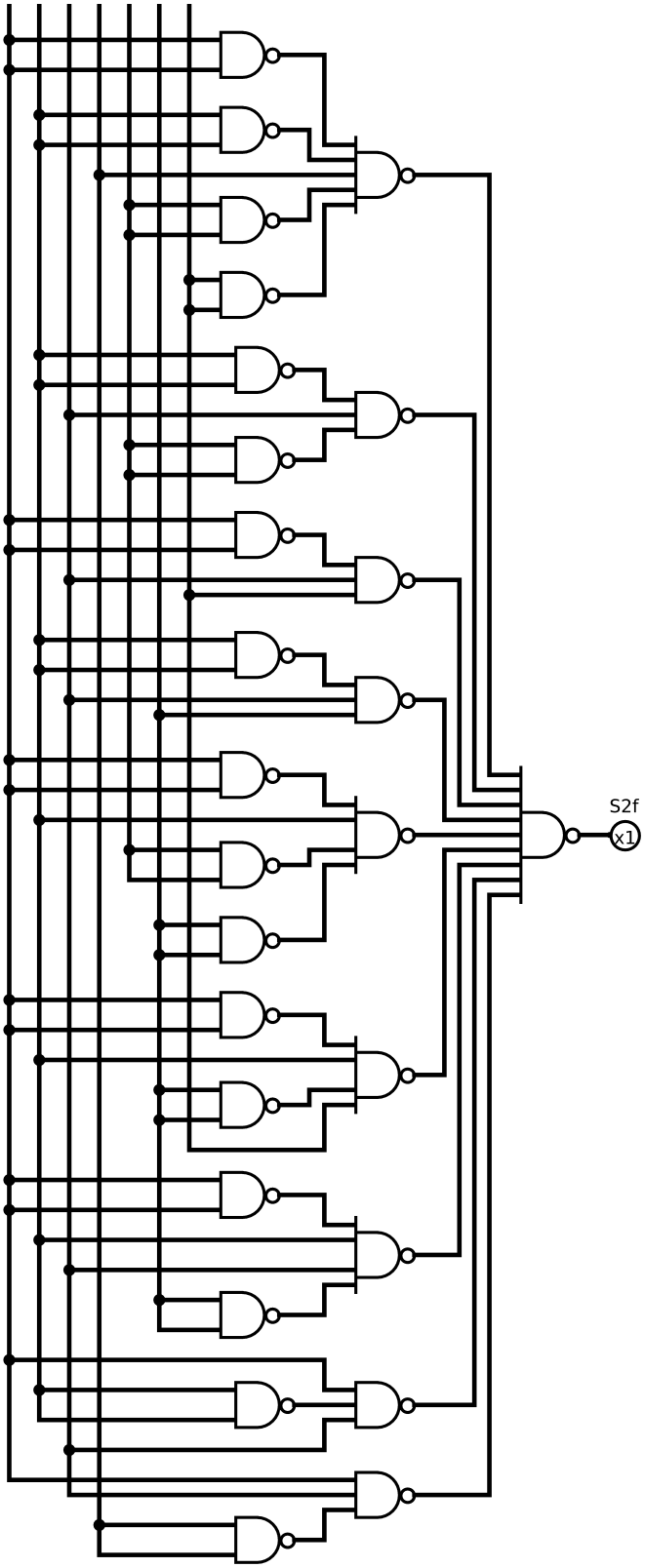

Figure 4.5: NAND gate realization of the input logic, continued from 4.4. Starting from the truth table the program *Logisim* built minimal logical expressions and converted them into the depicted NAND gate logic.

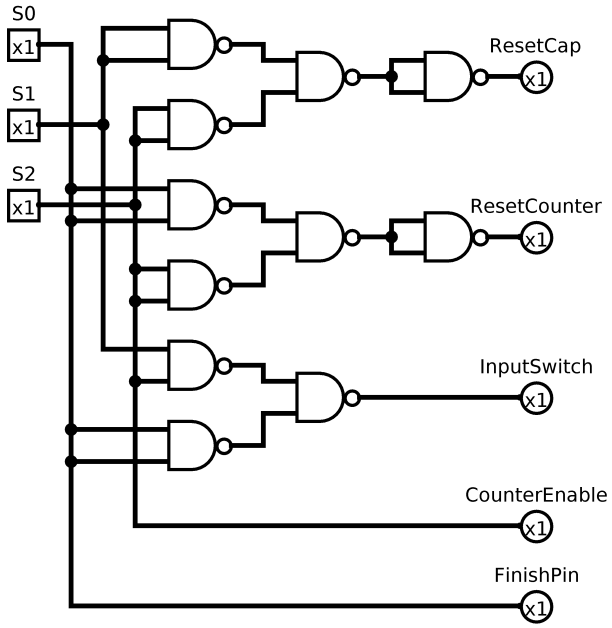

Figure 4.6: NAND gate realization of the output logic. Starting from the truth table the program *Logisim* built minimal logical expressions and converted them into the depicted NAND gate logic.

Integrator

The design presented in this work is based on the ones of Shan et al. mentioned above [11, 12], like shown in Figures 4.1, 3.3. Figure 4.7 shows the design of the included operational amplifier.

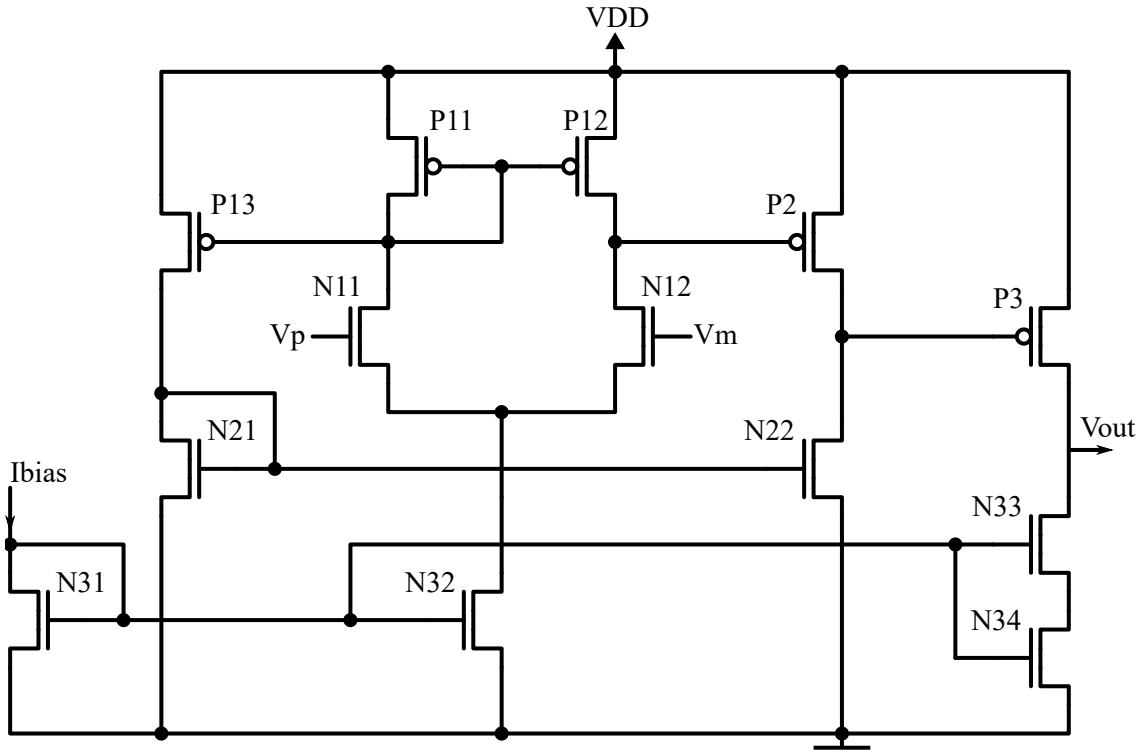

Figure 4.7: Designed MOSFET circuit realization of the operational amplifier. The supplied bias current I_{bias} has an amount of 10 nA and is mirrored to the differential input stage and the output stage paths to drastically limit the draining current. A second differential stage spun up by $P13$, $P2$, $N21$ and $N22$ further amplifies the input voltage difference. Notice that all MOSFETS shown are enhancement type FET's, bulks of NMOS transistors are always connected to *GND* and bulks of PMOS transistors are always connected to V_{dd}.

Comparator

The Comparator was already covered in another work (compare [5] page 36, Figure 2.14) at the same institute and work group in August 2017.

Counter

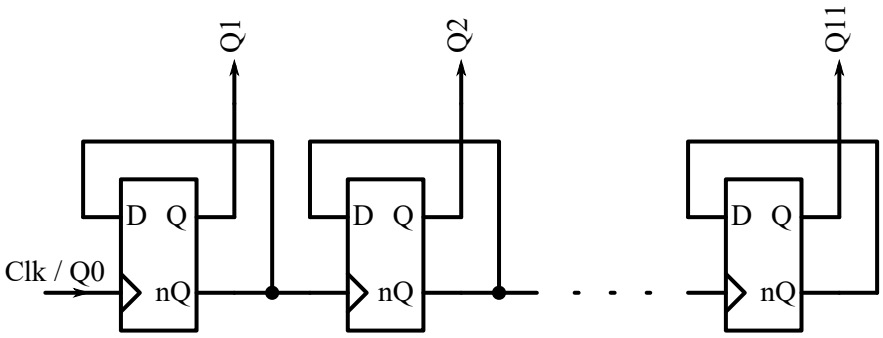

Figure 4.8: Assembly used for the realization of the 11 Bit counter. Due to the asynchronous design peak currents are reduced compared to a synchronous counter. The jitter induced by this design should have very little impact because of the relatively low operation frequency.

To realize an 11 bit asynchronous counter eleven D-flipflops are connected like shown in 4.8. The used fully static differential D-flipflop shown in Figure 4.9 is based on [16] (Figure 19) with the transistor parameters optimized for minimum current consumption at 2,1 MHz. An optimization took place because the current consumption of the initial design without tweaking transistor parameters was about 4 times higher. As this would have been more than 50% of the aimed maximum current consumption an optimization seemed desirable. Furthermore, a reset functionality is added using cmos mutual exclusion techniques.

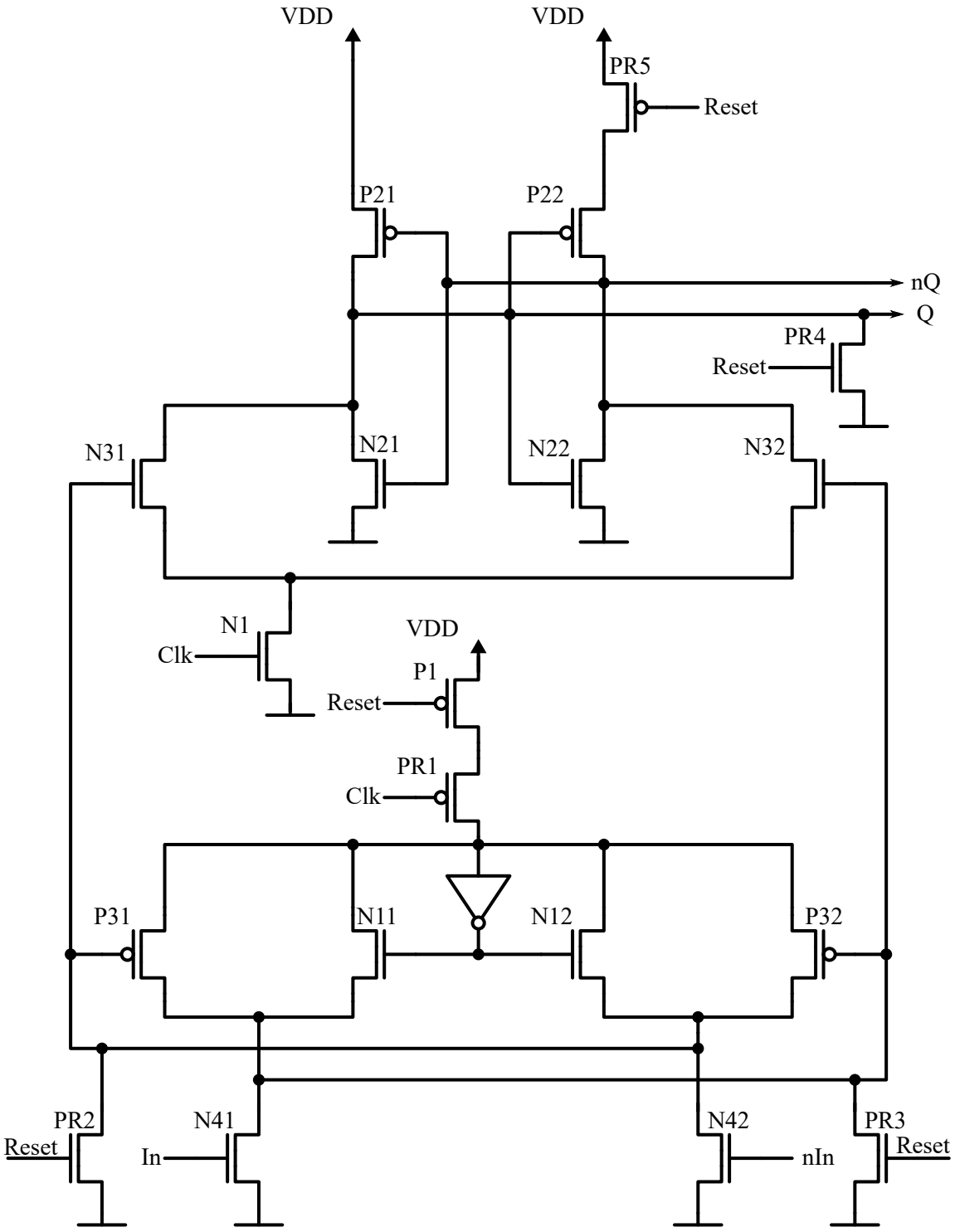

Figure 4.9: Implementation of the fully differential master slave D-flipflop with reset functionality. Notice that all MOSFETS shown are enhancement type FET's, bulks of NMOS transistors are always connected to *GND* and bulks of PMOS transistors are always connected to V_{dd}.

5 Simulation

The simulation restrains itself to the ADC core components as well as to the D-flipflop and thus to the counter accordingly as these appeared to be the most critical components regarding current consumption. The output signal quality of the ADC core components can be evaluated in Figure 5.2, while for the D-Flipflop it was part of the optimizational target function and, hence, is not further discussed here.

Simulation took place within the *Cadence ADE Assembler* where the generated results were directly transfered to the tables appearing in this chapter. The worst case overall current consumption of the ADC combined with the counter evaluates to 251,3 nA for the corner SS at 85 °C.

5.1 ADC core components

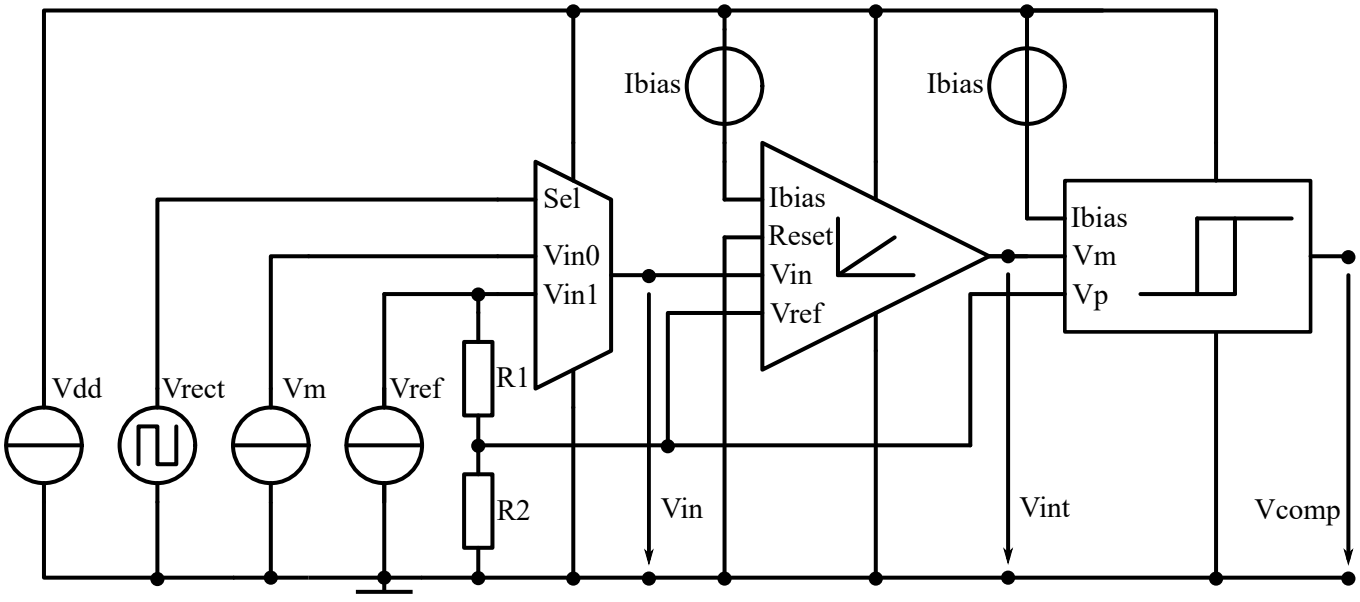

Figure 5.1: Testbench for current consumption and validation tests of the ADC's core components. A voltage V_m imitating the input signal's voltage level to convert is applied to compare with the theoretically evaluated behavior.

Different artificially generated constant measurement voltages 0, 0,35 V and 0,6 V were set for V_m (shown in Figure 5.1), the according average current consumption evaluated (Tables 5.1, 5.2, 5.3) and the integrators' loading and unloading curves plotted in Figure 5.2.

V_{rect} in this testbench just imitates the counter and parts of the state machine. It produces a 0 to 1 V step after the loading time has passed and therefore the mux switches V_{in} from V_m to V_{ref} measuring constant 0,7 V subsequently. The voltage divider $(R1, R2)$ derives the integrator and comparator reference voltage of 0,65 V. I_{bias} amounts, as always in this work, to 10 nA, V_{dd} to 1 V.

T in °C	Average current per corner in nA				
	FF	SS	FS	SF	TT
−40	119.9	103.9	120.6	102.2	111.6
0	125.1	109.3	125.6	107.8	116.9
85	139.1	120.1	142.8	118.6	128.6

Table 5.1: Average current consumption simulation results of the ADC core assembly of Figure 5.1 with $V_m = 0$ V. The maximum current consumption is shown highlighted.

T in °C	Average current per corner in nA				
	FF	SS	FS	SF	TT
−40	117.6	101.6	118.3	99.99	109.3
0	122.7	106.9	123.2	105.5	114.6
85	136.6	117.7	140.4	116.1	126.2

Table 5.2: Average current consumption simulation results of the ADC core assembly of Figure 5.1 with $V_m = 0{,}35$ V. The maximum current consumption is shown highlighted.

T in °C	Average current per corner in nA				
	FF	SS	FS	SF	TT
−40	115.9	100.3	116.6	98.71	107.8
0	121.1	105.3	121.4	103.9	112.9
85	134.8	115.9	138.6	114.2	124.4

Table 5.3: Average current consumption simulation results of the ADC core assembly of Figure 5.1 with $V_m = 0{,}6$ V. The maximum current consumption is shown highlighted.

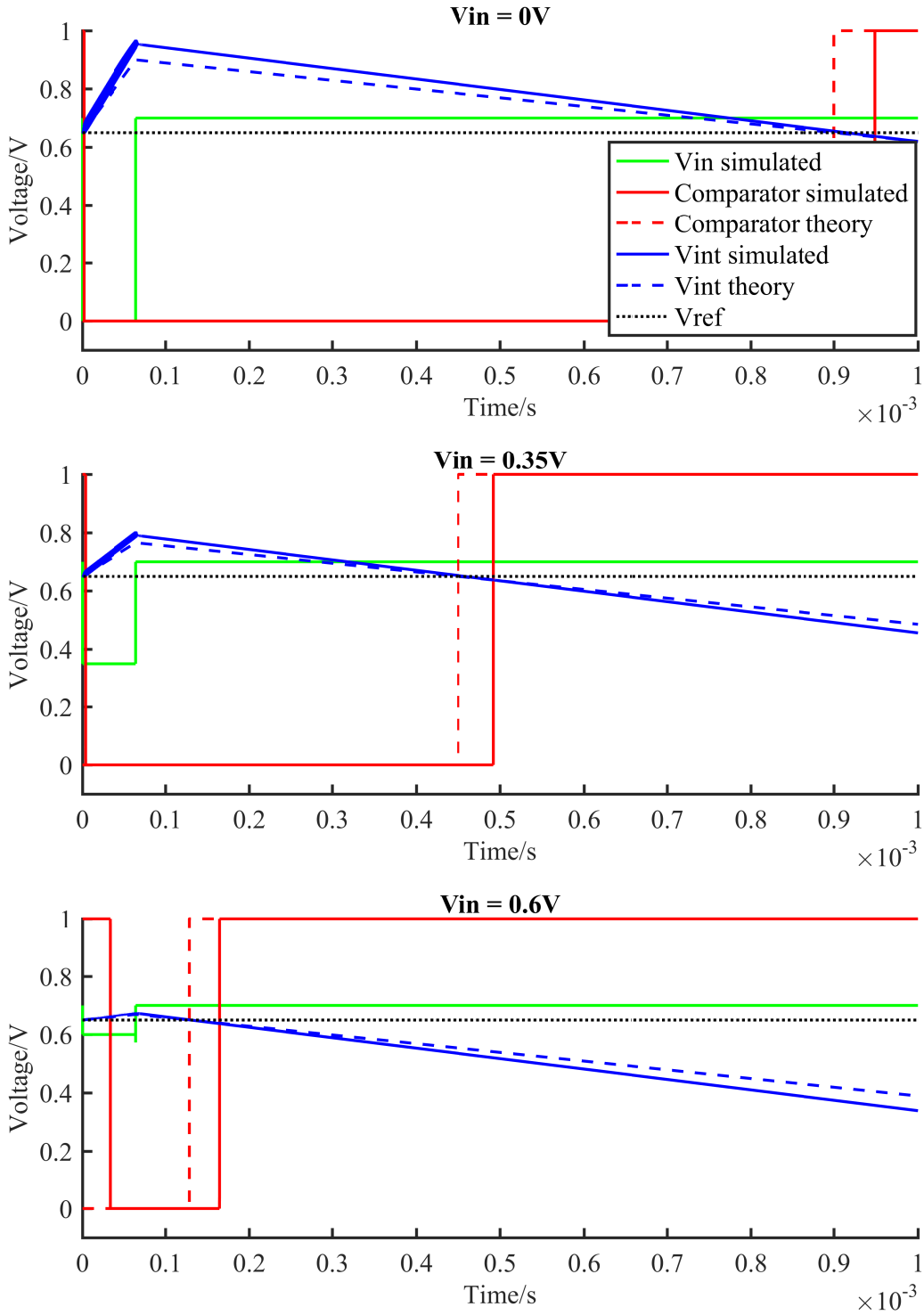

Figure 5.2: Comparison of theoretically calculated and simulated loading and unloading behaviors of the ADC for different constant input voltages V_m.

In Figure 5.2 the theoretically expected and simulated loading and unloading behavior of the integrator as well as the comparator switch characteristics can be observed. Especially with $V_{in} = 0$ one notices that the peak of V_{int} is higher than estimated, but the crossing point of simulated and calculated V_{int} with the reference voltage V_{ref} appears to be almost exactly at the same time, which can be explained well with a lack of accuracy regarding the component specifications of the resistor, the capacitor or the not evaluated parasitic resistances and the independence of the conversion output value to static electrical component specifications.

Regarding the comparator switching delay it has to be mentioned that the component taken from [5] has a hysteresis in scope of the switching behavior, which in this case is used constructively to avoid frequently occurring dynamic leakage currents. As the delay only depends on the temporal voltage level of V_{int} and therefore to its constant slope, the slope-depending bias can be subtracted. Furthermore, without a hysteresis the comparator would switch very often in a region where $V_{ref_{integrator}} \approx V_{int}$, which would produce higher dynamic current consumption, which is unwanted.

5.2 D-flipflop

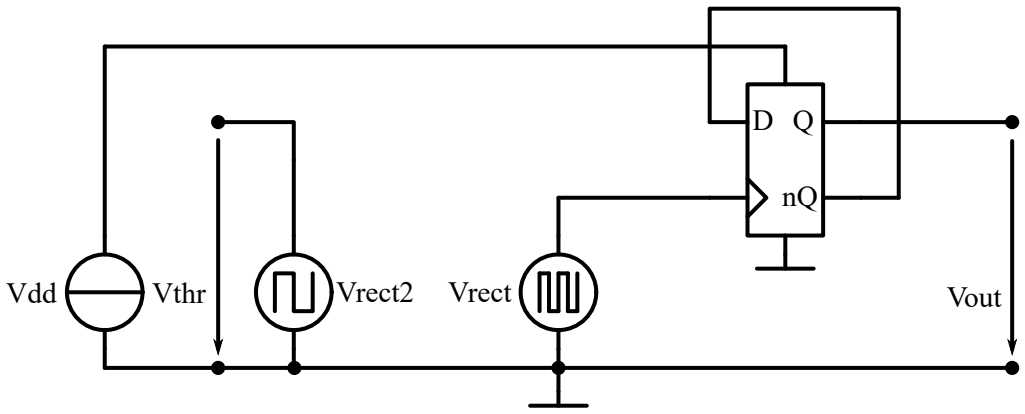

Figure 5.3: Testbench for optimizing the D-flipflop component presented in Figure 4.9. The optimization aims for two goals, the minimization of current consumption as well as for the correctness of the output signal. Thus, an ideal output signal form V_{thr} is artificially generated by V_{rect_2}.

The testbench depicted in Figure 5.3 is used for the optimization of the D-flipflop in terms of current consumption and signal correctness. The D-flipflop is connected to operate as 1 Bit counter.

T in °C	Average current per corner in nA				
	FF	SS	FS	SF	TT
−40	39.29	37.71	38.33	38.58	38.14
0	39.24	37.59	38.74	38.64	38.63
85	45.37	39.45	46.96	41.23	41.36

Table 5.4: Average current consumption simulation results of a single D-flipflop in the configuration of Figure 5.3. The maximum current consumption is shown highlighted.

T in °C	Average quadratic error per corner in mV				
	FF	SS	FS	SF	TT
−40	15.92	18.1	16.98	17.44	16.95
0	16.68	18.94	17.75	18.28	17.74
85	17.92	20.3	18.97	19.66	19.03

Table 5.5: Average quadratic error of the signal form compared to the ideal signal form of a single D-flipflop in the configuration of Figure 5.3. The maximum quadratic error is shown highlighted.

To cope with the signal shape the root mean square function is applied on the difference between the reference signal V_{rect2} and the simulated signal V_{rect} and set to become minimal in the scope of the optimizing simulation's target function. The reached minimum currents with respect to a correct signal shape for all temperature and process corners can be seen in Table 5.5.

5.3 Counter

The frequency of the rectangular periodic pulse generator, named V_{rect}, amounts to $f_{rect} = f_{0_{save}} = 2{,}1\,\text{MHz}$, the frequency of the rectangular periodic pulse generator, named V_{rect_2}, evaluates to $f_{rect_2} = \frac{f_{rect}}{2} = \frac{f_{0_{save}}}{2} = 1{,}05\,\text{MHz}$, which is the second counter D-flipflop's switching frequency. The third counter D-flipflop subsequently has a switching frequency of $f_{rect_3} = \frac{f_{rect_2}}{2} = \frac{f_{rect}}{4}$.

Assuming that the main current consumption of the D-flipflop comes from dynamic short circuit currents due to the mutual exclusion CMOS techniques applied to the design in Figure 4.9, coming to effect only when the D-flipflop switches, the overall current consumption for an $n+1$ bit counter can be estimated with the following sum.

For I_{dyn_1} the simulated worst case current consumption $I_{dyn_1} = 46{,}96\,\text{nA}$ of a single D-flipflop is taken into account.

$$I_{counter_{dyn}} = I_{dyn_1} + I_{dyn_2} + \cdots + I_{dyn_n} = \tag{5.1}$$

$$= I_{switch} f_{rect} + I_{switch} f_{rect_2} + \cdots + I_{switch} f_{r}ect_n = \tag{5.2}$$

$$= I_{switch} \frac{f_{rect}}{2^0} + I_{switch} \frac{f_{rect}}{2^1} + \cdots + I_{switch} \frac{f_{rect}}{2^n} \tag{5.3}$$

$$= I_{switch} f_{rect} \left(\frac{1}{2^0} + \frac{1}{2^1} + \cdots + \frac{1}{2^n} \right) = \tag{5.4}$$

$$= I_{dyn_1} \left(\frac{1}{2^0} + \frac{1}{2^1} + \cdots + \frac{1}{2^n} \right) \tag{5.5}$$

For higher values of n the sum inside the brackets converges to 2, hence, the frequency dependent worst-case current consumption of a counter with many bits should not be more than $I_{counter_{dyn}} \approx 2 \times 46{,}96\,\text{nA} = 93{,}92\,\text{nA}$. With static leakage currrents growing proportional to the number of D-flipflops the counters simulated worst-case current of 131,2 nA is very feasible.

T in °C	Average current per corner in nA				
	FF	SS	FS	SF	TT
−40	80.31	85.28	74.4	72.68	76.25
0	80.19	82.42	73.71	71.52	75.38
85	110.6	131.2	89.5	78.82	89.51

Table 5.6: Average current consumption simulation results of the eleven bit counter of Figure 4.1. The maximum current consumption is shown highlighted.

6 Layout

In this chapter the layouts derived from the schematics of chapter 4 are presented. The total chip area of the shown components measures $0{,}057\,306\,\mathrm{mm}^2$.

Many components are highly affected by process variations. Thus, measures to counter these problems are taken. The main strategy is to apply matching patterns like *common centroid* or *common source* to the sensible layout parts, especially on all current mirrors, all differential stages and even to the voltage divider.

To avoid parasitic capacitances and resistors as good as possible the layout and positioning process of the components aims less on saving chip area and more at shortening down copper trace lengths.

The layout in Figure 6.1 shows the physical implementation of the core components of the ADC including the voltage divider, a mux, a comparator an operational amplifier, the integrators resistor as well as it's charging capacitance.

Due to matching purposes the voltage divider is evenly split up into 28 resistors, where 2 of them are used for R_1 and 26 for R_2, that's why the depiction seems different from the integrator's resistor.

Figure 6.2 shows the counters D-flipflop cells stacked and hooked up like sketched in Figure 4.8. The design of a single cell is intended for optimal stackability. Thus, the ports are positioned accordingly.

The state machine layout depicted in Figure 6.3 consists of 3 fully static D-flipflops and nand gate layered input and output logics like shown in Figure 4.3. More place could be saved here, but as it is more of a goal to minimize copper traces' lengths to avoid incoupling voltages and currents due to higher trace capacitances and inductances.

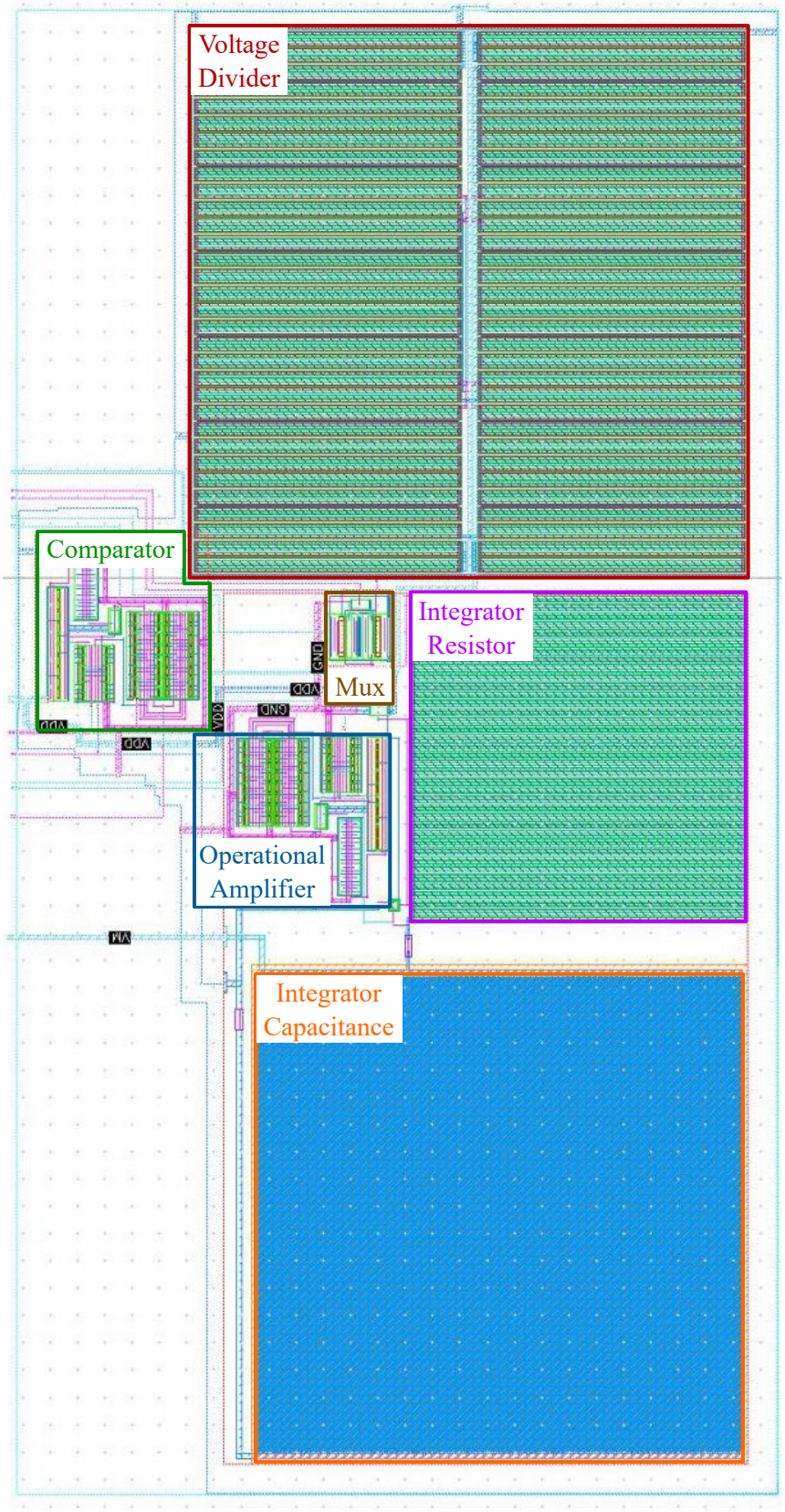

Figure 6.1: Layout of the Integrator with some peripheral components. The total area of these components amounts to 0,035 108 mm^2 and is spun up by a rectangle measuring 262 µm × 134 µm.

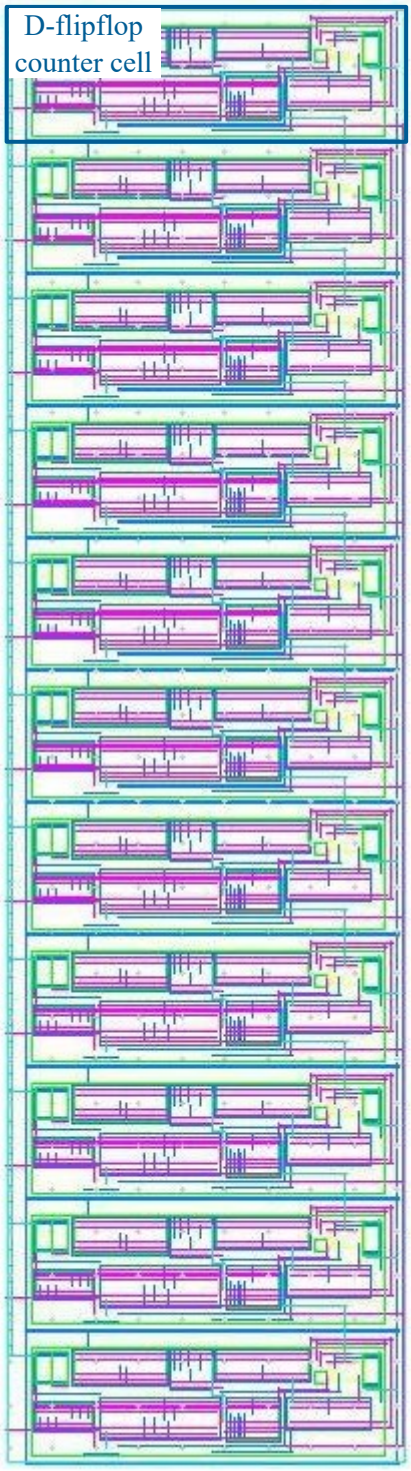

Figure 6.2: Layout of the counter sketched in 4.8. Single counter cells are designed to have an oblong outline shape to be able to be stacked adaptable. The total area of the counter component amounts to $0{,}011\,492\,\mathrm{mm}^2$ and is spun up by a rectangle measuring $68\,\mu\mathrm{m} \times 169\,\mu\mathrm{m}$.

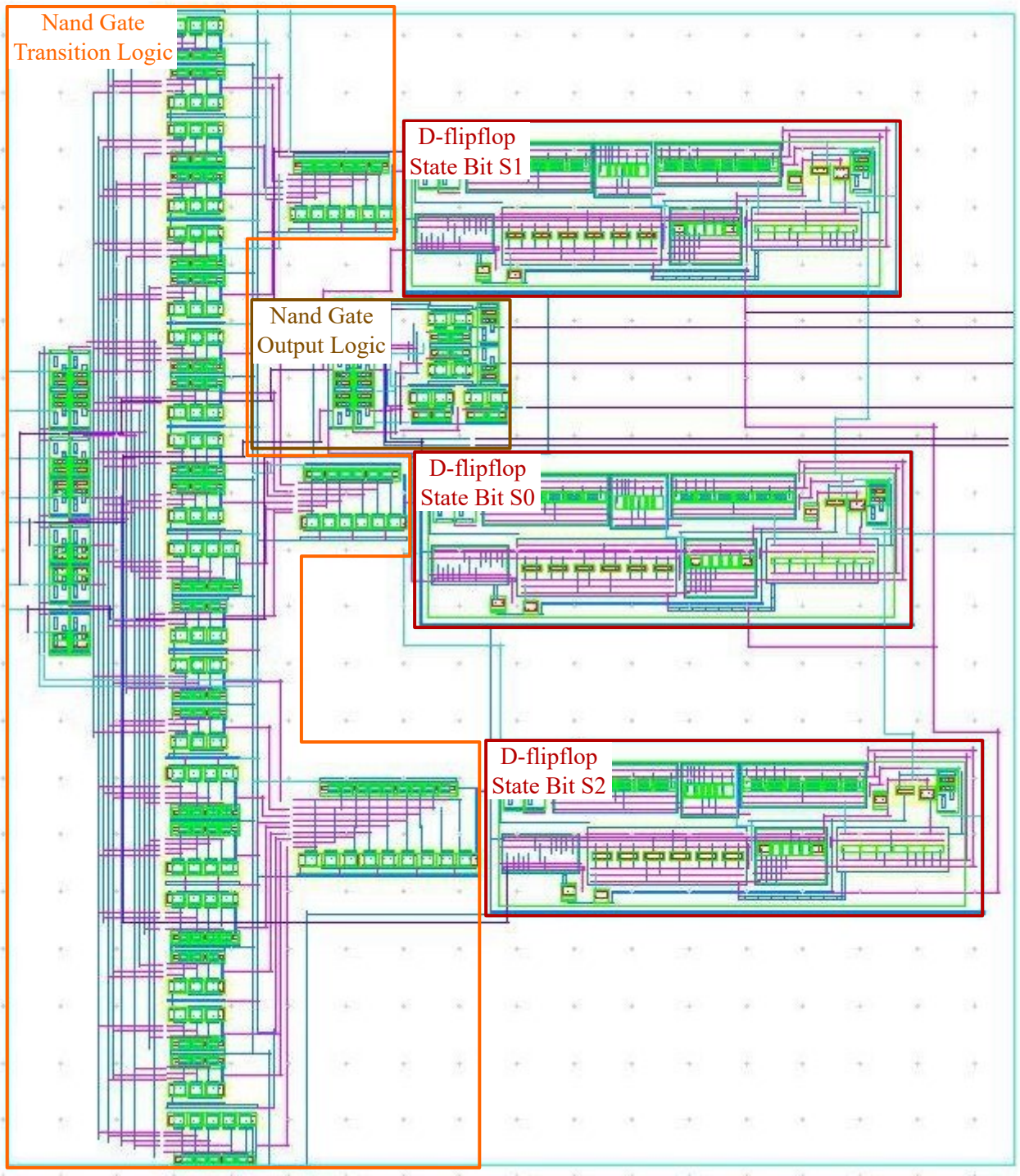

Figure 6.3: Layout of the state machine from Figure 4.3. The total area of the entire state machine component amounts to $0{,}010\,706\,\mathrm{mm}^2$ and is spun up by a rectangle measuring $106\,\mu\mathrm{m} \times 101\,\mu\mathrm{m}$.

7 Conclusion

As SensorBIM provided the possibility to research in the field of ultra low power analog-digital converters this work found very promising results which also can be widely used in other wireless sensing applications in the future. With a worst-case power consumption not higher than 300 nA which is less than a third of the originally estimated current consumption, it's now possible to either invest in better secondary ADC specifications or to directly interpret the power savings in tag range enhancement.

In this work not only the analog core parts of an ADC, namely the integrator but also the traditionally digitally designed parts, such as the state machine and the counter, are constructed analog. By minimizing their current consumption while ensuring the minimal functionality these components are expected to be more efficient (in terms of power) than their digitally designed counterparts. A comparison will be made in the future.

As this work shows the entire process of designing dual slope ADCs for ultra low power applications the next steps is to design appropriate sensors to be attached, to adapt the tag's digital core to properly work with the ADC, maybe replace the analog designed digital components with components of the digital core and to test the ADC for its quality of operation.

Appendix

Truth tables of the state machine

Internal truth table to depict the transition logic

S0	S1	S2	StartImpulse	BitQ9	Comparator	StopAndReset	S0f	S1f	S2f
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	1	1	0	0	0
0	0	0	0	1	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0
0	0	0	0	1	1	0	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	1	0	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	0	0	0	1
0	0	0	1	0	1	1	0	0	0
0	0	0	1	1	0	0	0	0	0
0	0	0	1	1	0	1	0	0	0
0	0	0	1	1	1	0	0	0	0
0	0	0	1	1	1	1	0	0	0
0	0	1	0	0	0	0	0	0	1
0	0	1	0	0	0	1	1	1	1
0	0	1	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1	1	1
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	0	1	1	1	1
0	0	1	0	1	1	0	1	1	1
0	0	1	0	1	1	1	1	1	1
0	0	1	1	0	0	0	0	0	1
0	0	1	1	0	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1
0	0	1	1	0	1	1	1	1	1
0	0	1	1	1	0	0	0	1	0
0	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	0	1	1	1

Table 1 continued from previous page

S0	S1	S2	StartImpulse	BitQ9	Comparator	StopAndReset	S0f	S1f	S2f
0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	1	1
0	1	0	0	0	0	1	1	1	1
0	1	0	0	0	1	0	1	1	0
0	1	0	0	0	1	1	1	1	0
0	1	0	0	1	0	0	0	1	0
0	1	0	0	1	0	1	1	1	1
0	1	0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	1	1	0
0	1	0	1	0	0	0	0	1	1
0	1	0	1	0	0	1	1	1	1
0	1	0	1	0	1	0	1	1	0
0	1	0	1	0	1	1	1	1	0
0	1	0	1	1	0	0	0	1	0
0	1	0	1	1	0	1	1	1	1
0	1	0	1	1	1	0	1	1	0
0	1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	0	0	1	1
0	1	1	0	0	0	1	1	1	1
0	1	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	1	1	1
0	1	1	0	1	0	0	0	1	1
0	1	1	0	1	0	1	1	1	1
0	1	1	0	1	1	0	1	0	0
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	0	0	1	1
0	1	1	1	0	0	1	1	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	0	1	1	1	1	1
0	1	1	1	1	0	0	0	1	1
0	1	1	1	1	0	1	1	1	1
0	1	1	1	1	1	0	1	0	0
0	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	0	0	0	1	0	1	0	0
1	0	0	0	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0	0
1	0	0	0	1	0	1	0	0	0
1	0	0	0	1	1	0	1	0	0
1	0	0	0	1	1	1	0	0	0
1	0	0	1	0	0	0	1	0	0
1	0	0	1	0	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0
1	0	0	1	0	1	1	0	0	0

Table 1 continued from previous page

S0	S1	S2	StartImpulse	BitQ9	Comparator	StopAndReset	S0f	S1f	S2f
1	0	0	1	1	0	0	1	0	0
1	0	0	1	1	0	1	0	0	0
1	0	0	1	1	1	0	1	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	0	0	0	0	1	1	1
1	0	1	0	0	0	1	1	1	1
1	0	1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	1	1	1
1	0	1	0	1	0	0	1	1	1
1	0	1	0	1	0	1	1	1	1
1	0	1	0	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1
1	0	1	1	0	0	0	1	1	1
1	0	1	1	0	0	1	1	1	1
1	0	1	1	0	1	0	1	1	1
1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	0	0	1	1	1
1	0	1	1	1	0	1	1	1	1
1	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	1	1	0
1	1	0	0	0	0	1	1	1	0
1	1	0	0	0	1	0	1	1	0
1	1	0	0	0	1	1	1	1	0
1	1	0	0	1	0	0	1	1	0
1	1	0	0	1	0	1	1	1	0
1	1	0	0	1	1	0	1	1	0
1	1	0	0	1	1	1	1	1	0
1	1	0	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0
1	1	0	1	0	1	0	0	0	0
1	1	0	1	0	1	1	0	0	0
1	1	0	1	1	0	0	0	0	0
1	1	0	1	1	0	1	0	0	0
1	1	0	1	1	1	0	0	0	0
1	1	0	1	1	1	1	0	0	0
1	1	1	0	0	0	0	1	1	1
1	1	1	0	0	0	1	1	1	1
1	1	1	0	0	1	0	1	1	1
1	1	1	0	0	1	1	1	1	1
1	1	1	0	1	0	0	1	1	1
1	1	1	0	1	0	1	1	1	1
1	1	1	0	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0

Table 1 continued from previous page

S0	S1	S2	StartImpulse	BitQ9	Comparator	StopAndReset	S0f	S1f	S2f
1	1	1	1	0	0	1	0	0	0
1	1	1	1	0	1	0	0	0	0
1	1	1	1	0	1	1	0	0	0
1	1	1	1	1	0	0	0	0	0
1	1	1	1	1	0	1	0	0	0
1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0

Table 1: State machhine Input Logic Table for moore automate presented in 4.2. The nand gate network depicted in figures 4.4 and 4.5 was realized by converting this table to a logical expression, minimizing and transforming it.

Truth table to depict the output logic

S0	S1	S2	ResetCap	ResetCounter	InputSwitch	CounterEnable	FinishPin
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0
0	1	1	0	0	1	1	0
1	0	0	1	0	1	0	1
1	0	1	x	x	x	x	x
1	1	0	0	0	1	0	1
1	1	1	0	0	1	0	1

Table 2: Statemachine output logic table for moore automate presented in 4.2. The nand gate network depicted in figure 4.6 was realized by converting this table to a logical expression, minimizing and transforming it.

Matlab Script for automated calculations

```
close all
%% Ultra Low Power Dual Slope ADC on GFs 55nm Design
   Process
%% Specifications
%% Frequencies
% Sampling Rate

fs = 1000 % Hz
%%
% Given Oscillator

fo_raw = 2.1E6 % Hz
%%
```

```
13 % To compensate for Jitter of Oscillator average Time
       over 2^3 = 8 ticks:
14
15 fo_save = 1
16 fo = fo_raw / fo_save
17 %% Time
18
19 Tmax = 1 / fs
20 Tpause = .1 * Tmax
21 % use 10% of Tmax to reset the cap and read the buffer
       etc.
22 %% Electrical
23
24 Vdd = 1 % V
25 Vref = .70 % V, temperature constant
26 Ibias = 1e-8 % 10nA
27 m = 2 % Multiplicity of IBIAS Mosfet
28 %%
29 % Temperature constant potential difference through
       Transdiode
30
31 Vref_bias_diff = 0.05 % V, exact, temperature constant
32 VrefIntegrator = Vref - Vref_bias_diff
33 %% Calculation
34 %% Time
35 % max unloading (Vunload - Vref) by max loading (Vref -
       Vload)
36 loadUnloadRatio = Vref_bias_diff/VrefIntegrator
37 Tconversion = Tmax - Tpause
38 Tload = Tconversion / (1/loadUnloadRatio + 1)
39 Tunload = Tconversion - Tload
40 loadBits = log2(Tload * fo)
41 %% Electrical
42
43 unloadBits = log2(Tunload * fo)
44 %% Counter
45
46 Bits = ceil(unloadBits)
47 CounterOverflowTime = 2^Bits * 1/fo
48 timeMargin = CounterOverflowTime - Tunload
49 %% Voltage Source Margin for Conversion Cap Maximum
       Voltage
50
51 Vdd_save = Vdd - 0.1
52 %% Electrical Component Specs
53
```

```
54 RC = Tload * VrefIntegrator / (Vdd_save - VrefIntegrator
   ) % Ohm * F
55 %% Load values for some Input Voltages
56
57 V0 = -1/RC * Tload * (0-VrefIntegrator) + VrefIntegrator
58 V035 = -1/RC * Tload * (0.35-VrefIntegrator) +
   VrefIntegrator
59 V06 = -1/RC * Tload * (0.6-VrefIntegrator) +
   VrefIntegrator
60 V07 = -1/RC * Tload * (0.7-VrefIntegrator) +
   VrefIntegrator
61 %%
62 % Resistances
63 %
64 % Measurement of the electrical parts:
65
66 RMeasurement = 5.02E6 % MOhm
67 BarsMeasurement = 40
68 LengthMeasurement = 70E-6 %um
69 BarSpacing = 0.25E-6 % um
70 MinWidth = 400E-9 %nm
71 resistancePerBarAndLength = RMeasurement / ...
72     (BarsMeasurement * LengthMeasurement)
73 %%
74 % Voltage Devider
75
76 Imax = 50E-9 % nA
77 RRatio = Vref_bias_diff/VrefIntegrator %
78 RGesMin = Vdd / Imax % Ohm
79 R1 = Vdd * RRatio / (Imax *(1+ RRatio))
80 R2 = R1 / RRatio
81 %%
82 % "opppcres" Part size for quadratic design
83
84 LengthR1 = sqrt(R1 * (BarSpacing + MinWidth) /
   resistancePerBarAndLength)
85 LengthR2 = sqrt(R2 * (BarSpacing + MinWidth) /
   resistancePerBarAndLength)
86 BarsR1 = LengthR1 / (BarSpacing + MinWidth)
87 BarsR2 = LengthR2 / (BarSpacing + MinWidth)
88 %%
89 % "opppcres" Part size for quadratic design
90 %
91 % ((*)2)2 ((A)2)8 ((B)2)1 ((A)2)10  ((B)2)1 ((A)2)8 ((*)
   2)2
92 %
```

```
93  % ((*)2)2 ((A)2)8 ((B)2)1 ((A)2)10  ((B)2)1 ((A)2)8 ((*)
        2)2
94
95  countA = (16*2+20)
96  countB = countA*RRatio
97  BarsPerInstance = 4
98  ResPerBar = RGesMin / ((countA + countB) *
        BarsPerInstance)
99  LengthPerInstance = ResPerBar / (
        resistancePerBarAndLength)
100 LengthPerInstanceMeasuredCadence = 99.646e-6
101 %%
102 % Integrator
103
104 R = 10e6 % Ohm
105 %%
106 % "opppcres" Part size for quadratic design
107 LengthIntegratorRes = ...
108     sqrt(R * (BarSpacing + MinWidth) /
            resistancePerBarAndLength)
109 BarsIntegratorRes = LengthIntegratorRes / (BarSpacing +
        MinWidth)
110 %%
111 % Cap
112
113 C = RC/R
114 %%
115 % Current Consumption of cap when loading
116
117 Iload = (VrefIntegrator - 0) / R
118 mLoad = Iload / Ibias
119 %%
120 % Appx. Current Consumption of overall when loading (
        from Simulation)
121
122 Ioverall = Iload * 1.03
123 %%
124 % Current Consumption of cap (must be provided by sensor
        ). Maybe think
125 % about an additional Inverting Input stage if sensor
        can't provide
126 % current.
127 %
128 % * unloading
129
130 Iunload = -Vref_bias_diff / R
131 %%
```

```
132 % Multiplicity of Current starved Inverter Transistor (
    Current Mirror)
133 % minimum Multiplicity for Unload Current Mirror,
    trimming down
134 % further results in higher peak voltages
135 mUnload = abs(Iunload) / Ibias * m
```

Listing 1: Matlab boilerplate code for designing dual slope ADCs

Bibliography

[1] Saima Bashir et al. „Analog-to-digital converters: A comparative study and performance analysis“. In: *Proceeding - IEEE International Conference on Computing, Communication and Automation, ICCCA 2016* (2017), pp. 999–1001. DOI: 10.1109/CCAA.2016.7813861.

[2] Klaus Bressler, Ekbert Hering, and Jürgen Gutekunst. *Elektronik für Ingenieure und Naturwissenschaftler*. 6. Auflage. Springer Vieweg. ISBN: 9783642054983. URL: https://link.springer.com/book/10.1007/978-3-642-05499-0.

[3] Francisco O.O. Gomes et al. „A low-power RFID enabled temperature sensor for cold chain management“. In: *Proceedings - IEEE International Symposium on Circuits and Systems* 2015-July (2015), pp. 2113–2116. ISSN: 02714310. DOI: 10.1109/ISCAS.2015.7169096.

[4] Ili Shairah Abdul Halim, Nor Syazwana Mohd Yusof, and Siti Lailatul Mohd Hassan. „A low power 0.18μm CMOS technology integrating dual-slope analog-to digital converter“. In: *IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE* (2014), pp. 317–320. DOI: 10.1109/SMELEC.2014.6920861.

[5] Christoph Happ. „Entwurf und Implementierung einer Ultra-Low-Power Empfängerschaltung für passive UHF RFID Transponder“. In: August 2017 ().

[6] Hao Chiao Hong, Long Yi Lin, and Chun Jung Liu. „Design of an on-scribe-line 12-bit dual-slope ADC for wafer acceptance test“. In: *Proceedings of the 2017 IEEE International Conference on Applied System Innovation: Applied System Innovation for Modern Technology, ICASI 2017* (2017), pp. 1751–1754. DOI: 10.1109/ICASI.2017.7988280.

[7] Walt Kester. „Which ADC architecture is right for your application II“. In: *Electronic Engineering Times* 1412 (2006), pp. 26–29. ISSN: 01921541.

[8] Man Kay Law, Amine Bermak, and Howard C. Luong. „A sub-μW embedded CMOS temperature sensor for RFID food monitoring application“. In: *IEEE Journal of Solid-State Circuits* 45.6 (2010), pp. 1246–1255. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2047456.

[9] Sechang Oh et al. „A dual-slope capacitance-to-digital converter integrated in an implantable pressure-sensing system“. In: *IEEE Journal of Solid-State Circuits* 50.7 (2015), pp. 1581–1591. ISSN: 00189200. DOI: 10.1109/JSSC.2015.2435736.

[10] Georg Saxl et al. „55 nm Ultra-Low-Power Local Oscillator for EPCglobal Gen2v2 Standardized Passive UHF RFID Tags“. In: *IEEE MTT-S International Microwave Symposium Digest* 2018-June (2018), pp. 942–945. ISSN: 0149645X. DOI: 10.1109/MWSYM.2018.8439478.

[11] Hengying Shan et al. „A low power CMOS temperature sensor frontend for RFID tags“. In: *SIRF 2018 - 2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* 2018-Janua (2018), pp. 15–18. DOI: 10.1109/SIRF.2018.8304217.

[12] Hengying Shan et al. „A low power programmable dual-slope ADC for single-chip RFID sensor nodes“. In: *SiRF 2017 - 2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2017), pp. 118–120. DOI: 10.1109/SIRF.2017.7874388.

[13] Bo Wang et al. „A passive RFID tag embedded temperature sensor with improved process spreads immunity for a -30C to 60C sensing range“. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.2 (2014), pp. 337–346. ISSN: 15498328. DOI: 10.1109/TCSI.2013.2278388.

[14] Heemin Y Yang and Rahul Sarpeshkar. „A Time-Based Energy-Efficient Analog-to-Digital Converter“. In: 40.8 (2005), pp. 1590–1601.

[15] Teng Yang et al. „Compact and Supply-Voltage-Scalable Temperature Sensors for Dense On-Chip Thermal Monitoring“. In: *IEEE Journal of Solid-State Circuits* 50.11 (2015), pp. 2773–2785. ISSN: 00189200. DOI: 10.1109/JSSC.2015.2476815.

[16] Jiren Yuan and Christer Svensson. „New single-clock CMOS latches and flipflops with improved speed and power savings“. In: *IEEE Journal of Solid-State Circuits* 32 (1997), pp. 62–69. URL: https://ieeexplore.ieee.org/abstract/document/553179/.

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